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Patents ADP Number *(if you know it)*

If the applicant is a corporate body, give the country/state of its incorporation — THE NETHERLANDS

4. Title of the invention — ACTIVE MATRIX DISPLAY DEVICES

5. Name of your agent *(if you have one)*
"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*

PAUL LEWIS WILLIAMSON
Philips Intellectual Property and Standards
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Country	Priority Application number *(if you know it)*	Date of filing *(day/month/year)*

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Number of earlier application	Date of filing *(day/month/year)*

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11. I/We request the grant of a patent on the basis of this application.

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DESCRIPTION

ACTIVE MATRIX DISPLAY DEVICES

This invention relates to active matrix electro-optic display devices comprising an array of pixels addressed via sets of address conductors, and particularly to active matrix liquid crystal display devices (AMLCDs). The invention is concerned more especially with active matrix display device circuit arrangements and methods of operation for addressing groups of two or more pixels or sub-pixels within the array.

Conventionally, AMLCDs comprise a row and column array of pixels which are connected to, and addressed via, sets of row and column address conductors. The pixels of one row are usually connected to the same row address conductor while each pixel in the row is connected to a respective, and different, column address conductor. An example of such a device, its method of operation, and its method of fabrication is described in US-A-5130829 to which reference is invited and whose contents are incorporated herein.

Such display devices are widely used in a variety of products, including for example lap-top computers, PDAs and mobile phones and other portable electronic equipment. Full colour display devices are now becoming more common in relatively small products such as mobile phones. Also, for portability, these products tend to rely on batteries for their power.

It is desirable for display devices intended for use in mobile phone applications and the like to have a very low power consumption in order to conserve battery power. However, there is increasing interest in integrating video functions into mobile devices which means that they must also have good grey scale capability. It is difficult to satisfy both of these requirements at the same time and therefore display devices have been proposed which can be operated in two different modes, a relatively high power, full grey scale, mode and a low power mode which has reduced grey scale capability.

One technique for reducing the power consumption of the display device is to operate it in an 8 colour mode in which the red, green and blue

pixels of the display device are driven to one of two states, a light state in which the transmission or reflection of the pixel is high and a dark state in which the transmission or reflection is low. This method of operating the display device offers a reduced power consumption because the circuitry, such as digital to analogue converters, which is required to generate the drive voltages for the grey scales can be put into an inactive low power state.

This low power operating mode can be extended to offer increased grey scale and colour capability by dividing the pixels of the display into sub pixels. These sub pixels can be given different areas, for example a pixel may consist of two sub pixels one having an area A and a second having an area 2A. By independently driving these sub pixels to the dark state or the light state the display can be operated to produce 64 colours and 4 grey levels with only a moderate increase in power consumption compared to the 8 colour operation.

Examples of AMLCDs using this area-ratio grey-scale sub-pixellation approach are described, for example, in US 6,335,778 B1 and US 2002/0047822A1, whose contents are incorporated herein as reference material.

Dividing each pixel into a number of sub pixels raises the issue as to how these additional sub pixels should be addressed. Figure 1 illustrates one approach to addressing the additional sub pixels, similar to the kind of approach described in US 2002/0047822A1, each sub pixel, P1 to P4, is addressed in a similar way to a conventional pixel. A respective TFT is connected between each sub-pixel and a common adjacent column address conductor. Additional row address conductors are provided so that each sub pixel can be separately addressed with drive voltages applied to the column conductor. Examples of the row addressing waveforms are shown in Figure 1a. A disadvantage of this addressing technique is that the capacitance of the column conductor will be increased by both the capacitance of the additional TFTs connected to it and the capacitance of the crossovers with the additional row conductors.

The present invention provides circuit arrangements for the pixels, and methods of operating such, enabling addressing groups of two or more (sub)

pixels which results in a lower column capacitance. The circuit arrangements are compatible with operation of the display device in a low power stand by mode with reduced colour and grey-scale capability, for example 64 colours, and in a video mode with a full grey scale capability.

Various novel concepts, inventive concepts and specific embodiments are disclosed herein, particularly, but not exclusively, with reference to the accompanying drawing Figures 2 to 8.

In accordance with one aspect of the invention, a plurality of pixels or sub pixels are addressed through a common TFT (thin film transistor) which is connected to a column address conductor.

This has the advantage that the capacitance of the column address conductor is reduced compared to the arrangement of Figure 1. When the display device is operated in the video mode this common TFT can be used to control the simultaneous charging of the sub pixels. In the low power operating mode additional TFTs are used to allow different data to be applied to the sub pixels.

This and other advantageous features in accordance with the present invention are illustrated specifically in embodiments of various and different aspects of the invention now to be described, by way of example, with reference to the accompanying drawing figures, in which:-

Figure 1 shows schematically a possible circuit of a typical pixel, comprising a plurality of sub-pixels, in an AMLCD.

Figure 1a shows schematically example waveforms for operating the AMLCD of Figure 1;

Figure 2 shows schematically the circuit configuration of a typical pixel, comprising a plurality of sub-pixels, in an embodiment of AMLCD according to the present invention;

Figure 3 shows schematically the circuit configuration of a typical pixel, comprising a plurality of sub-pixels, in another embodiment of AMLCD according to the present invention;

Figures 4 and 5 illustrate schematically waveforms used in the driving of the devices of Figures 2 and 3 respectively;

Figure 6 shows schematically the circuit configuration of part of the pixel array, comprising a plurality of pixels in adjacent rows and columns, in a further embodiment of AMLCD in accordance with the present invention; and

Figures 7 and 8 illustrate respectively schematically waveforms used in the driving of the device of Figure 6 in first and second modes of operation.

Referring to Figure 2, there is shows a part of a first embodiment of AMLCD in accordance with the invention, comprising a typical pixel consisting of a plurality, in this case four, sub pixels, P1-P4.

The sub pixels are connected in a serial manner. Each sub pixel P1 to P4 is connected to the output terminal of a respective TFT switch with the input terminal of the TFT switch being connected to the preceding sub pixel. The TFT switch associated with the first sub pixel, P1, is connected to the column electrode. Data voltage signals for each of the sub pixels are supplied through this single column conductor. Each TFT switch has a separate control (gating) signal which is supplied via a row conductor.

In the second example embodiment illustrated in Figure 3, the sub pixels are connected in a parallel manner. Again each sub pixel P1 to P4 is connected to the output terminal of a switching TFT but in this case the input terminals of all TFTs except that associated with the first sub pixel P1 are connected to the first sub pixel. As before each TFT has a separate control signal supplied via a row conductor.

Both of these pixel circuit configurations have the advantage that they can readily be addressed in the two modes which correspond to the low power mode and video mode described previously.

In the low power mode of operation different video information must be applied to each of the sub pixels. This is achieved by supplying the information sequentially to the column conductor and by applying appropriate switching waveforms to the row conductors. The waveforms required by the two example circuits of Figures 2 and 3 are different and are illustrated in Figures 4 and 5, respectively.

In the case of the first example embodiment of Figures 2 and 4, the sub pixels must be charged sequentially, starting with P4 and ending with P1. This is achieved by using the overlapping row addressing pulses shown in Figure 4. In the case of the second example embodiment of Figures 3 and 5, the TFT switches associated with all sub pixels apart from the first are selected sequentially while the first TFT is held in a conducting state. Finally the first sub pixel is charged and then the first TFT is turned off.

In the video mode of operation the same drive voltage is applied to all of the sub pixels P1 to P4. This can be achieved by holding the associated row conductors, rows n+1 to n+3, at a voltage which turns on the TFT switches. Row n is then driven with conventional row selection waveforms, the row voltages being switched to a select (gating) voltage level in order to turn on the TFT connected to the column conductor and to charge all sub pixels simultaneously and then returned to a non-select voltage level in order to turn off this TFT and to isolate the sub pixels from the column electrode.

It is possible to reduce the number of row conductors required to address the display device by using a modified pixel circuit and modified row addressing waveforms. An example of part of an array which makes use of the addressing scheme proposed here is shown in Figure 6. In this example pixels X+1 and X+2, X+3 and X+4, X+5 and X+6 etc. represent pairs of sub pixels in a display device which provides for a 64 colour low power operating mode by dividing the area of each pixel into two area ratioed sub pixels.

In the low power mode, where the sub pixels must be addressed with different information, the array is scanned from top to bottom using the row addressing waveforms shown in figure 7. In order to address the sub pixels X+2, X+4, X+6, X+8 etc. The row electrode below the pixel must be taken to a select level. In order to address the sub pixels X+1, X+3, X+5, X+7 etc. both the row conductor above and the row conductor below the pixel must be taken to the select voltage level.

Since taking one of the row conductors to the select voltage level will affect both the row of pixels above and below the selected row conductor it is important that the rows are addressed in the correct sequence so that

information applied to a particular sub pixel is not corrupted when a subsequent sub pixel is being addressed.

Figure 7 indicates the operations that are being performed on each of the sub pixels during each period of the addressing sequence. There are three types of operation: 1) Charging, when the sub pixel is connected to the column conductor via the switching TFTs and is charged to the voltage present on the column conductor. 2) Charge sharing, when The TFT between a pair of the sub pixels is turned on and charge sharing takes place between the capacitances of the sub pixels, the sub pixels are isolated from the column conductor. 3) Holding, the voltage is maintained on the capacitance of the sub pixels.

The sequence in which the sub pixels are addressed is chosen so that after a sub pixel has been charged to the required drive voltage level it will not undergo any further charge sharing or charging operation until shortly before it is re-addressed in the following field period.

In the video operating mode the same video information must be applied to pairs of sub pixels. This is achieved using the addressing waveforms shown in Figure 8. In this mode the display device must be scanned in the reverse direction, from bottom to top, in order to avoid disturbing the pixel voltage after it has been addressed.

Although the above description is concerned with addressing groups of sub pixels within a pixel of the display device the approach could also be applied to addressing groups of pixels which are not sub pixels. This would allow the column capacitance of high resolution displays to be reduced.

Although described in relation to AMLCDs in particular, it is envisaged that the invention may be applied to active matrix display devices using electro-optic materials other than LC material, for example electrophoretic material.

From reading the present disclosure, many other modifications will be apparent to persons skilled in the art. Such modifications may involve other features which are already known in the art and which may be used instead of or in addition to features already described herein. No specific patent claims

have yet been formulated in the application to particular combinations of features, and it should be understood that the scope of the disclosure of the present application includes any and every novel feature or combination of features disclosed herein either explicitly or implicitly and together with all such modifications and variations, whether or not relating to the main inventive concepts disclosed herein and whether or not it mitigates any or all of the same technical problems as the main inventive concepts. The applicants hereby give notice that patent claims may be formulated to such features and/or combinations of such features during the prosecution of the present application or of any further application derived or claiming priority therefrom.

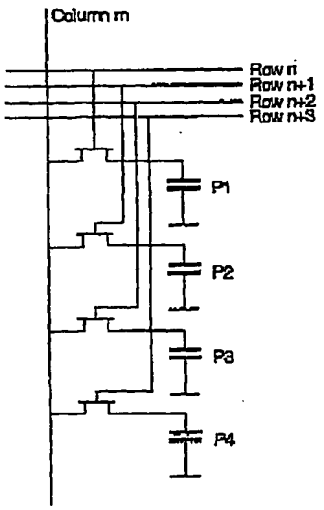
Column m
Row n
Row n+1
Row n+2
Row n+3
P1
P2
P3
P4

Fig. 1.

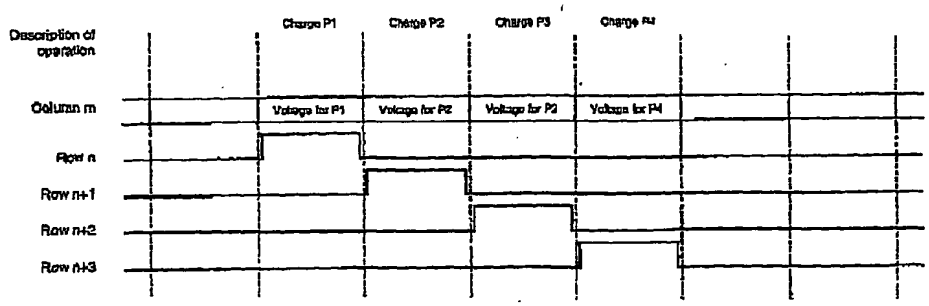
Description of operation
Charge P1
Charge P2
Charge P3
Charge P4
Column m
Voltage for P1
Voltage for P2
Voltage for P3
Voltage for P4
Row n
Row n+1
Row n+2
Row n+3

Fig. 1a

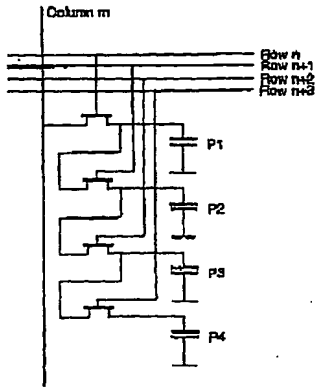

Fig. 2

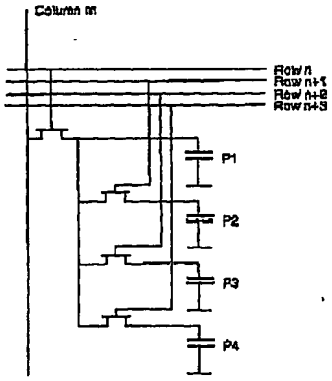

Fig. 3

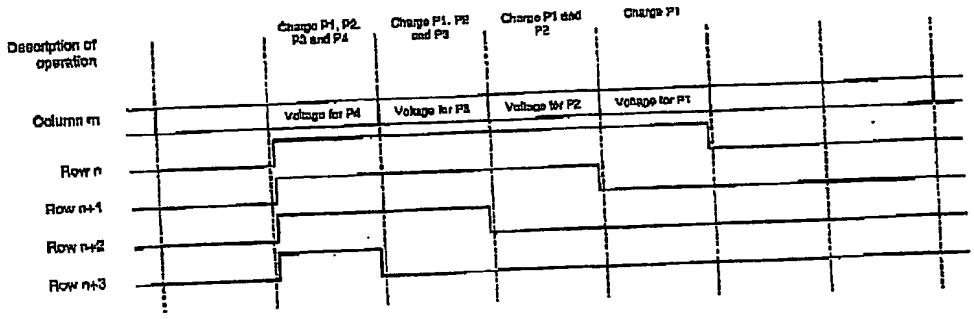
Description of operation
Charge P1, P2, P3 and P4
Charge P1, P2 and P3
Charge P1 and P2
Charge P1
Column m
Voltage for P4
Voltage for P3
Voltage for P2
Voltage for P1
Row n
Row n+1
Row n+2
Row n+3

Fig. 4.

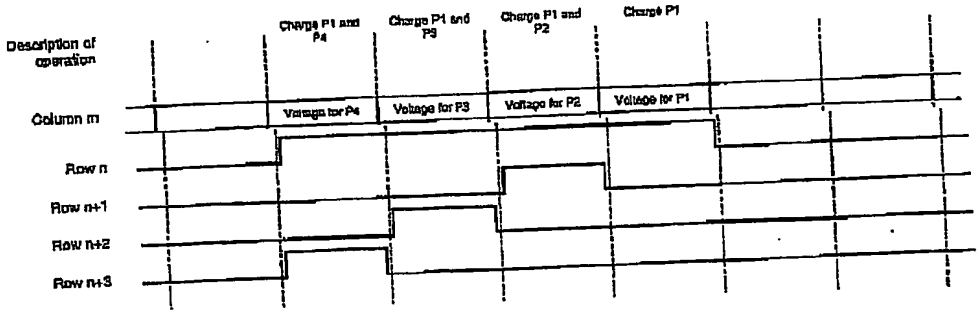
Description of operation
Charge P1 and P4
Charge P1 and P3
Charge P1 and P2
Charge P1
Column m
Voltage for P4
Voltage for P3
Voltage for P2
Voltage for P1
Row n
Row n+1
Row n+2
Row n+3

Fig. 5.

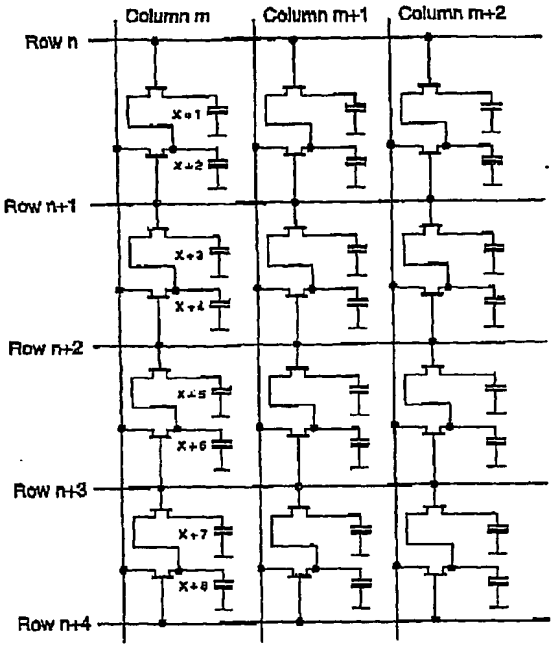

Fig. 6.

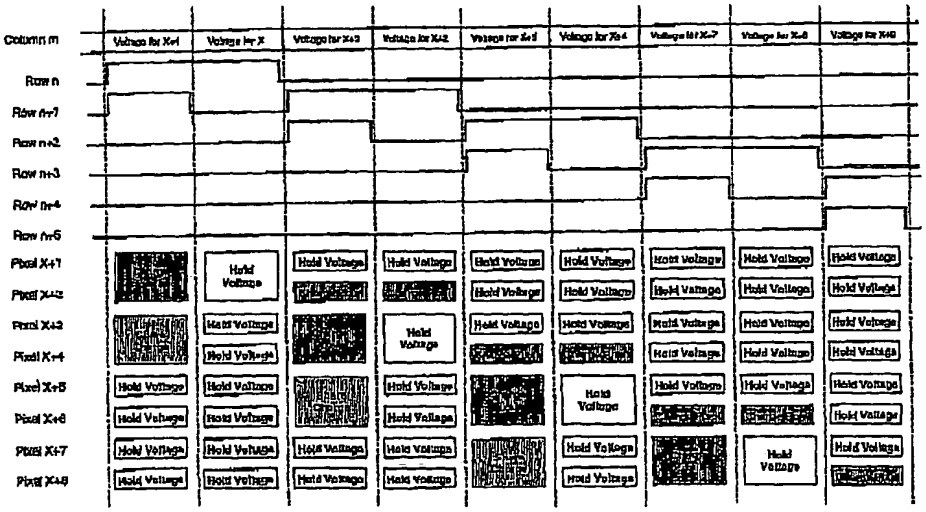

Fig. 7.

PHGB 020156

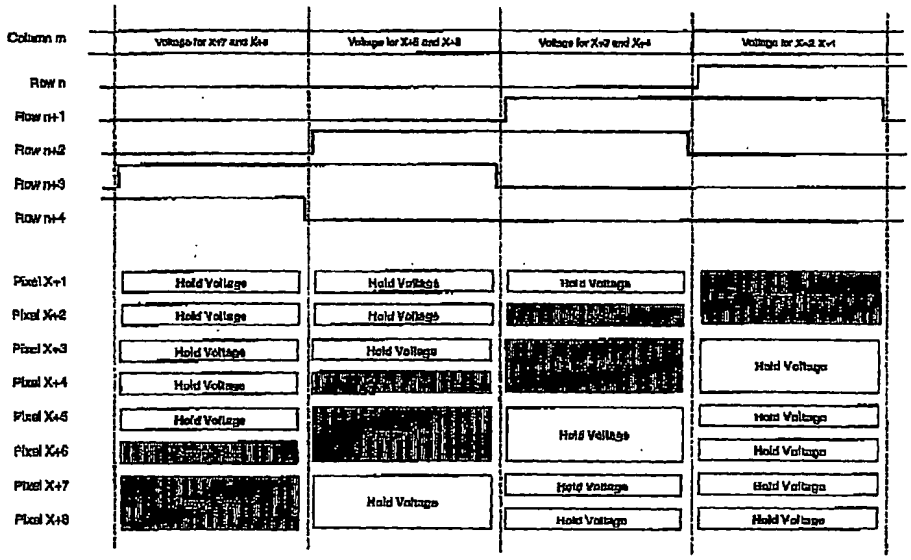
Column m
Row n
Row n+1
Row n+2
Row n+3
Row n+4
Pixel X+1
Pixel X+2
Pixel X+3
Pixel X+4
Pixel X+5
Pixel X+6
Pixel X+7
Pixel X+8
Hold Voltage

Fig. 8.

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